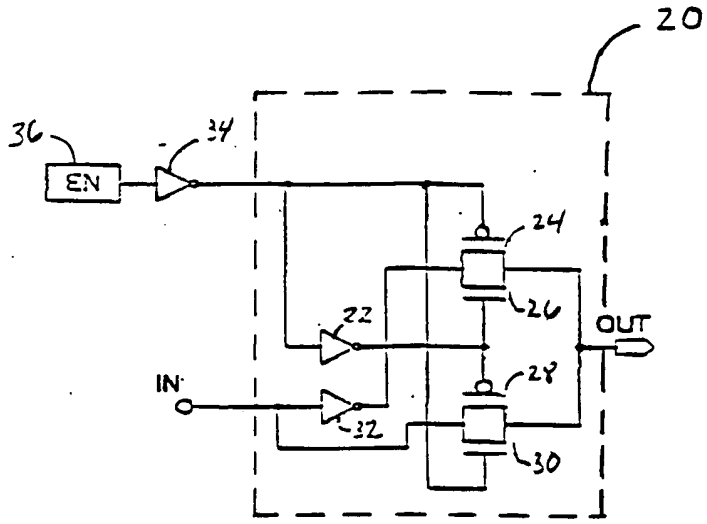
VERSION WITH MARKINGS TO SHOW CHANGES MADE

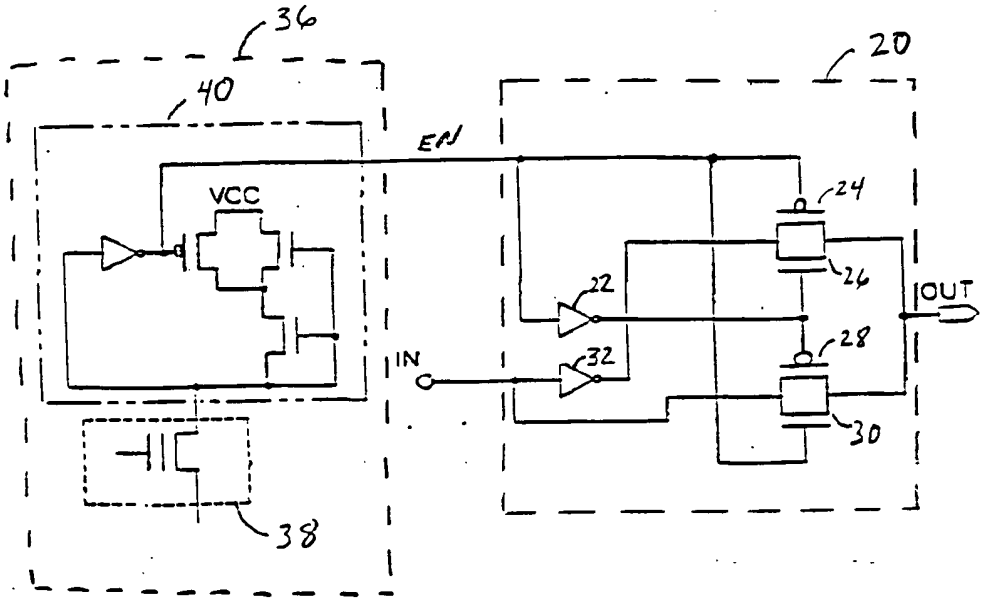
Please replace the paragraph beginning on page 14, line 19 with the following paragraph:

Referring to FIG. 9, a schematic diagram illustrating an implementation of the circuit 220 of FIG. [6] 8 is shown. The memory cells 222 and 224 may be implemented in accordance with the transistor circuit described in connection with FIG. 5.



Conventional

FIG. 1



Conventional

FIG. 2